CLAIM AMENDMENTS

1. (Previously Amended) A digital multiplication apparatus adopting redundant binary arithmetic for multiplying a number X by an m-bit number Y to produce a product, using a radix-2k number system, the apparatus comprising:

a data converter for data-converting the m-bit number Y into m/k-digit data D (= $D_{m/k-1}D_{m/k-2}$ .... D_i ... D_iD_o);

a partial product calculator for converting each of the digits Di of the m/k-digit data D converted by the data converter into a combination of coefficients of a fundamental multiple, multiplying the combination by the number X, to produce redundant binary partial products;

a redundant binary adder for summing the redundant binary partial products for each of the m/k-digit data D to produce a redundant binary sum; and

a redundant binary (RB)-normal binary (NB) converter for converting the redundant binary sum into a normal binary number and outputting the normal binary sum as the product of the two numbers X and Y.

2. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 1, wherein the partial product calculator comprises:

a fundamental multiple determiner for dividing the number Y into upper bits and lower bits by recoding the number Y, determining the sum of the products of the divided lower bits by corresponding weighted values to be the coefficient of the fundamental multiple, determining the product of the sum of the products of the divided upper bits by corresponding weighted values by 2^k to be the coefficient of a the fundamental multiple, and multiplying the determined coefficients of the fundamental multiple by the number X and outputting the product as the fundamental multiple;

first through m/k-th multiplexers;

first through m/k-th logic combination units; and

a controller for receiving all of the digits of the number Y converted by the data converter, producing the combination of the coefficients of the fundamental multiple with

respect to each digit D_i, and generating selection signals according to the produced combination, wherein each of the multiplexers selects two among the fundamental multiples in response to the selection signals, and the logic combination units perform logic combinations on the fundamental multiples selected by the multiplexers and output the results of the logic combinations as the redundant binary partial products to the RB-NB converter.

3. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 2, wherein each of the logic combination units comprises:

a first inverter for inverting one of the two selected fundamental multiples;

a second inverter for inverting the other fundamental multiple;

a first exclusive OR unit for performing an exclusive OR operation on the output of the first inverter and an n-th bit from the least significant bit of the number Y; and

a second exclusive OR unit for performing an exclusive OR operation on the output of the second inverter and the most significant bit of the number Y, wherein the results of the exclusive OR operations by the first and second exclusive OR units are the redundant binary partial products.

4. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 3, wherein each of the logic combination units further comprises:

a first inversion OR unit for performing an inversion OR operation on the outputs of the first and second exclusive OR units;

a first AND unit for performing an AND operation on the outputs of the first and second exclusive OR units; and

a second inversion OR unit for performing an inversion OR operation on the output of the first AND unit and the output of the first inversion OR unit.

5. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 3, wherein the redundant binary adder comprises first through

$\log_2\left(\left\lceil \frac{m}{k}+1 \right\rceil\right)$ redundant binary adding ports, each of the redundant binary adding ports has a predetermined number of adders, each of the adders adds two redundant binary partial products (a_i^+, a_i^-) and (b_i^+, b_i^-) using the following logic combination formula to obtain (d_i^+, d_i^-):

$$d_i^+ = \left(f_i \oplus h_{i-1}\right)\cdot\left(\overline{f_{i-1}}\cdot k_{i-1} + f_{i-1}\cdot h_{i-2}\right) \equiv \alpha_i \cdot \overline{\beta_{i-1}}$$

$$d_i^- = \overline{\left(f_i \oplus h_{i-1}\right)}\cdot\left(\overline{f_{i-1}}\cdot\overline{k_{i-1}} + f_{i-1}\cdot\overline{h_{i-2}}\right) \equiv \overline{\alpha_i}\cdot\beta_{i-1}$$

$$\left[\begin{array}{l} here,\ f_i = \left(a_i^+ \oplus a_i^-\right) \oplus \left(b_i^+ \oplus b_i^-\right) \\ h_i = a_i^+ \cdot \overline{a_i^-} + b_i^+ \cdot \overline{b_i^-} \\ k_i = \overline{\left(a_i^+ \oplus a_i^-\right)} + \left(a_i^+ \cdot \overline{a_i^-}\right) + \left(b_i^+ \cdot \overline{b_i^-}\right) \end{array}\right]$$

6. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 5, wherein each of the adders comprises:

a third inversion OR unit for performing an inversion OR operation on the output of the second inversion OR unit of the corresponding logic combination unit and a previous carry parameter h_{i-1};

a second AND unit for performing an AND operation on the output of the second inversion OR unit of the corresponding logic combination unit and the previous carry parameter h_{i-1};

a fourth inversion OR unit for performing an inversion OR operation on the output of the third inversion OR unit and the output of the second AND unit;

a fifth inversion OR unit for performing an inversion OR operation on the result of the previous inversion OR operation by the third inversion OR unit and the output of the fourth inversion OR unit;

a third AND unit for performing an AND operation on the result of the previous inversion OR operation by the third inversion OR unit and the output of the fourth inversion OR unit; and

a sixth inversion OR unit for performing an inversion OR operation on the output of the fifth inversion OR unit and the output of the third AND unit, wherein the output of the fifth inversion OR unit is $d_i^+ \cdot \overline{d_i^-}$, and the output of the sixth inversion OR unit is $\overline{d_i^+ \oplus d_i^-}$.

7. (Original) The digital multiplication apparatus adopting a redundant binary arithmetic of claim 5, wherein each of the adders comprises:

a fourth AND unit for performing an AND operation on the output of the first inversion OR unit of a logic combination unit and the output of the first inversion OR unit of another logic combination unit;

a seventh inversion OR unit for performing an inversion OR operation on the inputs of the fourth AND unit;

an eighth inversion OR unit for performing an inversion OR operation on the output of the fourth AND unit and the output of the second inversion OR unit of the former logic combination unit;

a third inverter for inverting the output of the second inversion OR unit of the former logic combination unit;

a complementary MOS inverter installed between the output of the second inversion OR unit of the former logic combination unit and the output of the third inverter, for receiving and inverting the output of the second inversion OR unit of the latter logic combination unit;

a fourth inverter for inverting the output of the complementary MOS inverter;

a first transmission gate for transmitting the input of the complementary MOS inverter to the fourth inverter in response to the output of the second inversion OR unit of the former logic combination unit and the output of the third inverter;

a fifth inverter for inverting the previous output of the seventh inversion OR unit;

a second transmission gate for transmitting the output of the fifth inverter in response to the output of the fourth inverter and the output of the complementary MOS inverter;

a third transmission gate for transmitting the previous output of the seventh inversion OR unit in response to the output of the complementary MOS inverter and the output of the fourth inverter;

a fourth transmission gate for transmitting the previous output of the seventh inversion OR unit in response to the output of the fourth inverter and the output of the complementary MOS inverter;

a fifth transmission gate for transmitting the output of the eighth inversion OR unit in response to the output of the complementary MOS inverter and the output of the fourth inverter;

a ninth inversion OR unit for performing an inversion OR operation on the outputs of the second and third transmission gates and the previous outputs of the fourth and fifth transmission gates;

a fifth AND unit for performing an AND operation on the inputs of the ninth inversion OR unit; and

a tenth inversion OR unit for performing an inversion OR operation on the output of the fifth AND unit and the output of the ninth inversion OR unit, wherein the output of the ninth inversion OR unit is $d_i^+ \cdot \overline{d_i^-}$, and the output of the tenth inversion OR unit is $\overline{d_i^+ \oplus d_i^-}$.

Claims 8-12 (Cancelled).